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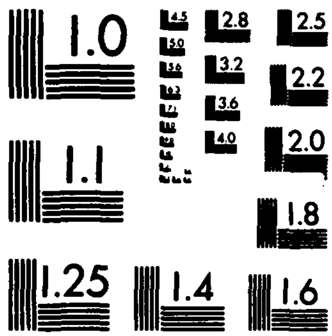

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Formation of MOS Gates by Rapid Thermal/Microwave Remote Plasma Multiprocessing

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Abstract

A novel cold-wall single-wafer lamp-heated Rapid Thermal/Microwave Remote Plasma Multiprocessing (RTMRPM) reactor has been developed for multilayer *in-situ* growth and deposition of dielectrics, silicon, and metals. This equipment is the result of an attempt to enhance semiconductor processing equipment versatility, to improve process reproducibility and uniformity, to increase growth and deposition rates at reduced processing temperatures, and to achieve *in-situ* multiprocessing in conjunction with real-time process monitoring and automation. For high-performance MOS VLSI applications, a variety of selective and nonselective tungsten deposition processes were investigated in this work. The tungsten gate MOS devices fabricated using the remote plasma multiprocessing techniques exhibited negligible plasma damage and near-ideal electrical characteristics. The flexibility of the reactor allows optimization of each process step yet allows multiprocessing.

Introduction

Future technological advancements in integrated electronics will require development of flexible custom fabrication technology for custom VLSI systems. Low temperatures and short times are essential requirements of future VLSI processing and the use of plasma processing in conjunction with single-wafer lamp heating in a flexible environment is a major step to realize this goal. As demonstrated in this work, the combination of single-wafer rapid thermal processing and microwave remote plasma can provide a powerful multipurpose reactor for VLSI device fabrication. *In-situ* multiprocessing reduces contamination, enhances circuit yield, and makes the formation of numerous new device structures feasible. The multipurpose capabilities of rapid thermal processing (RTP) have already been established through its application to silicon epitaxial growth [1], and *in-situ* fabrication of silicon gate MOS capacitors [2].

Reproducible growth of thin dielectrics in hot-wall furnaces is difficult due to long ambient and temperature transient times and constant furnace temperatures. Since furnaces are designed for multiwafer processing, extensive *in-situ* real-time measurements are difficult to perform. Rapid thermal oxidation and nitridation (RTO and RTN) of silicon in oxygen and ammonia ambients has already been recognized as an attractive technique for the growth of silicon nitride, silicon dioxide, nitrided oxides, oxidized nitrides, and application-specific (composition-tailored) insulators [3]. We have also demonstrated the feasibility of low-temperature nitridation of silicon in nitrogen plasma remotely generated by microwave discharge [4]. Among other growth and deposition processes, LPCVD of tungsten has emerged as a viable technology for VLSI applications such as MOS gate electrodes [5], low resistivity contacts and contact barriers, multilevel interconnections, and reduction of source/drain parasitic resistance. The conventional hot-wall LPCVD furnaces are not appropriate for reproducible high-rate tungsten deposition and nonselective formation of tungsten on insulators. This paper presents results on application of this

multiprocessing technique to deposite tungsten layers for semiconductor integrated circuit technologies.

Multiprocessing Reactor Design

Based on our experiences with remote microwave plasma nitridation and the rapid thermal dielectric growth and anneal processes, we have developed a novel cold-wall single-wafer *Rapid Thermal/Microwave Remote Plasma Multiprocessing* (RTMRPM) reactor for *in-situ* growth and deposition of dielectrics, silicon, and metals. The reactor design is so comprehensive that several processing steps can be sequentially done *in situ*, at the same time the reactor is highly flexible allowing optimization of each processing step. This reactor is expected to enhance equipment versatility, to improve process reproducibility and uniformity, to increase growth and deposition rates, and to achieve *in-situ* semiconductor multiprocessing. Figure 1 shows the schematic of the simplified prototype design employed to obtain the preliminary results presented in this letter. The water-cooled stainless steel chamber provides various ports for gas injection, optical heating of the wafer, vacuum pumping, and *in-situ* process monitoring. The wafer sits on low thermal mass quartz pins facing the end cone of a discharge tube and is heated on the other side by arrays of tungsten-halogen lamps (multiple discharge tubes are employed in the final reactor design). The optical flux reaches the wafer through a water-cooled quartz window. The wafer temperature can be controlled in a range from room temperature to 1150°C for seconds up to many minutes.

The gas distribution network for the RTMRPM reactor consists of three gas manifolds and any permissible combinations of a variety of gases (Ar, Ne, N_2, O_2, NH_3, NF_3, forming gas, N_2O, HCl, SF_6, WF_6, heated WCl_6 solid source, H_2, SiH_4, GeH_4, and SiF_4) can be injected into the chamber either through a quartz tube at the bottom of the chamber or through the side port nonplasma injectors. Remote plasma can be generated inside the tube by a microwave discharge cavity operating at 2450 MHz (S band). In contrast to the

conventional localized plasma techniques, the remote microwave plasma approach allows selective and controlled generation of specific plasma species simultaneous with injection of additional nonplasma gases into the process chamber without having to deal with the complications arising from the gas discharge in a composite gas ambient. The availability of remote plasma processing not only allows low-temperature dielectric growth and LPCVD of insulators and silicon epitaxy but also has enabled us to develop several new processes for nonselective deposition of tungsten and its compounds (e.g. nitrides) on insulating layers for MOS gate applications. This system configuration is very flexible for *in-situ* multiprocessing because it allows rapid cycling of ambient gases, temperature, and plasma with negligible cross-contamination and process memory effects. As a result, this reactor is expected to lead in a new direction towards flexible computer-aided manufacturing (CAM) of custom VLSI circuits.

Tungsten Deposition Processes

The main objective of our initial efforts was to develop reliable processes for *in-situ* fabrication of tungsten-gate MOS devices which requires the growth of gate dielectric by RTO and RTN cycles followed by a nonselective tungsten deposition process to form the gate electrode. Tungsten is quite attractive as an MOS gate material [7]; however, a reliable process for *in-situ* formation of tungsten gate electrodes has not been developed. Recently, blanket tungsten films were deposited on SiO_2 films at substrate temperatures below 450°C by photo-enhanced and microwave plasma-enhanced (hydrogen plasma) CVD techniques [8]. Tungsten-gate MOS VLSI can be realized if some of the major problems related to the poor adhesion of tungsten to insulating layers, channeling of implanted dopants through tungsten gate, lack of oxidation resistance, and gate dielectric degradation [9] are overcome. We have used two approaches to solve this problem: one by using a silicon glue layer [10] and the other by the use of RTMRPM technology.

As a result of the process limitations of the silicon glue technique [10], a variety of selective and nonselective processes were investigated in this work. Table 1 presents a summary of the tungsten deposition processes developed using our multiprocessing reactor. These techniques are grouped based on the plasma condition and the injection mode of various ambient gases. The depositions were studied extensively in a wide range of gas flows, pressure, and substrate temperature. A number of these nonselective processes are reported for the first time in this work. When WF_6 or a mixture of WF_6+H_2 was injected through the nonplasma port, generation of H_2 plasma, Ar plasma, or Ar+H_2 plasma in the quartz tube promoted nonselective tungsten deposition on insulating surfaces. Addition of Ar to H_2 enhances the plasma emission intensity and density of available atomic hydrogen. Another nonselective deposition technique developed in this work employed WF_6+Ar plasma along with nonplasma H_2. Under appropriate experimental conditions none of these nonselective deposition techniques caused tungsten deposition on the chamber walls or inside the quartz tube. The mixture of NH_3+H_2 and WF_6 always resulted in nonselective deposition for both plasma and nonplasma types of processes. Moreover, the combination of N_2+H_2 plasma and WF_6 also resulted in nonselective metallic film deposition. The films deposited by any of the last three techniques in Table 1 (rows J,K,L) had higher resistivities compared to pure tungsten and were expected to be tungsten nitride compounds. The surface morphology and stability of the CVD tungsten nitrides were functions of the deposition technique and experimental conditions. Tungsten nitride may exhibit useful properties such as oxidation resistance, diffusion barrier, and ion implant channeling stop. Tungsten nitride films could also be formed by RTN of tungsten layers. The films nitrided at the highest temperature (1000°C or more) were powdery; however, the tungsten films nitrided at lower temperatures (e.g. 825°C) were stable. According to the Auger depth profiles the films nitrided at 825°C and above were tungsten oxynitrides. Good *in-situ* adhesion to insulators was obtained for nonselectively deposited tungsten films thicker than 1 μm.

In some instances, one initial tungsten deposition cycle was followed by another type of deposition in order to obtain optimal adhesion and uniformity properties.

Any combination of $WF_6/H_2/Ar$ without plasma discharge (rows A through E in Table 1) resulted in very selective tungsten depositions on exposed silicon areas. The selective depositions were performed in a wide range of gas flow rates, pressure, and temperature and selectivity was maintained for depositions well over 1 μm. Compared to a furnace, this single-wafer cold-wall reactor offers a much larger processing window for selective processes without loss of selectivity after long times at elevated temperatures as much as 450°C. SiF_4 is known to retard the silicon reduction reaction of WF_6. Selectivity was also preserved in a mixture of $WF_6/H_2/SiF_4$ even at temperatures as high as 650°C. This indicated that in contrast to SiH_4, SiF_4 cannot initiate nonselective tungsten deposition even at very high deposition temperatures. The mixture of H_2 and SiF_4 did not result in any silicon deposition at temperatures as high as 650°C.

All of the nonselective deposition techniques developed in this work are applicable to *in-situ* fabrication of metal gate MOS devices. Various MOS devices were successfully fabricated using these techniques. As an example, Fig. 2 plots the high-and low-frequency capacitance-voltage (C-V) characteristics of MOS devices with RTMRPM-deposited tungsten gates and without any final forming gas anneal. Nearly 300 Å thick gate oxide was grown in a furnace in dry oxygen ambient at 950°C for 60 min followed by 60 min Ar anneal at the same temperature. In these particular devices, the initial tungsten nucleation on gate oxide was promoted by a plasma deposition process (row G in Table 1) and this cycle was followed by a nonplasma deposition cycle (row E in Table 1) to make the film thicker. As indicated by the C-V characteristics, the devices exhibit respectable performance and negligible plasma damage. The oxide thickness measured by ellipsometry (308 Å) and extracted from the C-V data (303 Å) were similar which implies that no reduction of SiO_2 has occurred during the initial plasma deposition cycle. Assuming negligible fixed oxide

charge density, the flatband voltage value (0.54 V) indicates that the gate work function is located near the silicon midgap which is what should be expected from tungsten and should be ideal for NMOS as well as PMOS devices. The surface-state density distribution plotted in Fig. 3 shows a midgap value of 6×10^{10} $eV^{-1}cm^{-2}$. This value is relatively low for an unannealed MOS device. There may have been a possibility of some hydrogen annealing during the tungsten deposition process.

Summary

In conclusion, this novel rapid thermal/remote microwave plasma multiprocessing technique has potential merits for *in-situ* fabrication of future high-performance MOS VLSI circuits.

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Table 1: Various types of plasma and nonplasma tungsten LPCVD processes developed in the novel RTMRPM reactor.

TUNGSTEN DEPOSITION PROCESSES				
Deposition Type	Gases through the Quartz Tube	Gases through the Side Ports	Microwave Power	Deposition Condition
A	None	WF_6+Ar	OFF	Selective
B	None	WF_6+H_2	OFF	Selective
C	Ar	WF_6+H_2	OFF	Selective
D	SiF_4	WF_6+H_2	OFF	Selective
E	H_2	WF_6	OFF	Selective
F	H_2	WF_6	ON	Nonselective
G	Ar+H_2	WF_6	ON	Nonselective
H	Ar	WF_6+H_2	ON	Nonselective
I	WF_6+Ar	H_2	ON	Nonselective
J	N_2+H_2	WF_6	ON	Nonselective
K	NH_3+H_2	WF_6	ON	Nonselective
L	NH_3+H_2	WF_6	OFF	Nonselective

Figure Captions

Figure 1. Schematic of the novel cold-wall single-wafer lamp-heated rapid thermal/microwave remote plasma multiprocessing (RTMRPM) reactor.

Figure 2. High-frequency (100 KHz) and Low-frequency (50 mV/sec) capacitance-voltage characteristics of MOS devices with furnace-grown gate oxide and tungsten gate electrode deposited by RTMRPM. The average flatband voltage across the wafer is 0.537 V (0.096 V standard deviation).

Figure 3. Surface-state density distribution of tungsten-gate MOS devices with the C-V characteristics shown in Fig. 2. The average midgap D_{it} across the wafer is 6.03×10^{10} $eV^{-1}cm^{-1}$ (0.61×10^{10} $eV^{-1}cm^{-2}$ standard deviation).

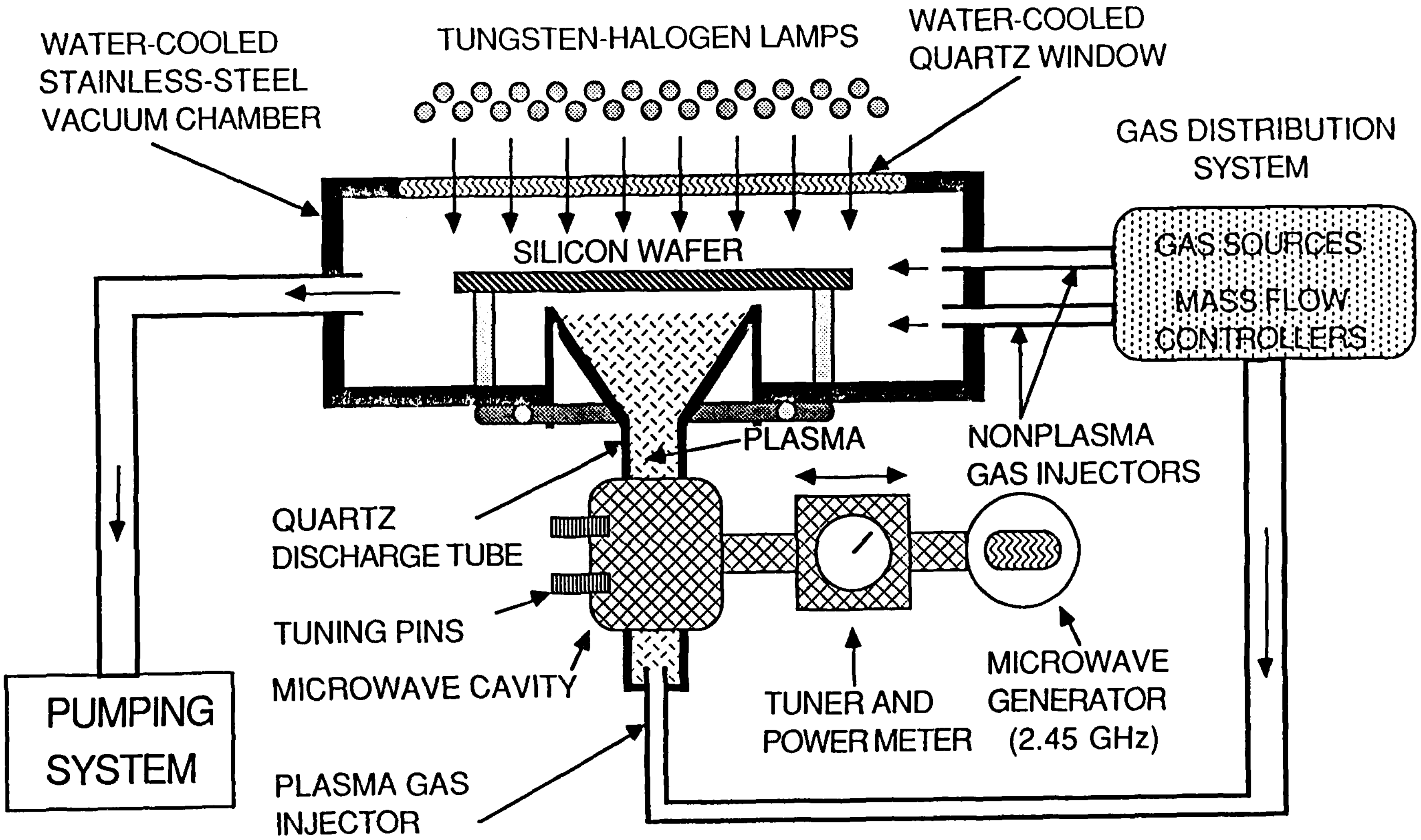
WATER-COOLED
STAINLESS-STEEL
VACUUM CHAMBER
TUNGSTEN-HALOGEN LAMPS
WATER-COOLED
QUARTZ WINDOW
GAS DISTRIBUTION
SYSTEM
SILICON WAFER
GAS SOURCES
MASS FLOW
CONTROLLERS
PLASMA
NONPLASMA
GAS INJECTORS
QUARTZ
DISCHARGE TUBE
TUNING PINS
MICROWAVE CAVITY
PUMPING
SYSTEM
TUNER AND
POWER METER
MICROWAVE
GENERATOR
(2.45 GHz)
PLASMA GAS
INJECTOR

Figure 1

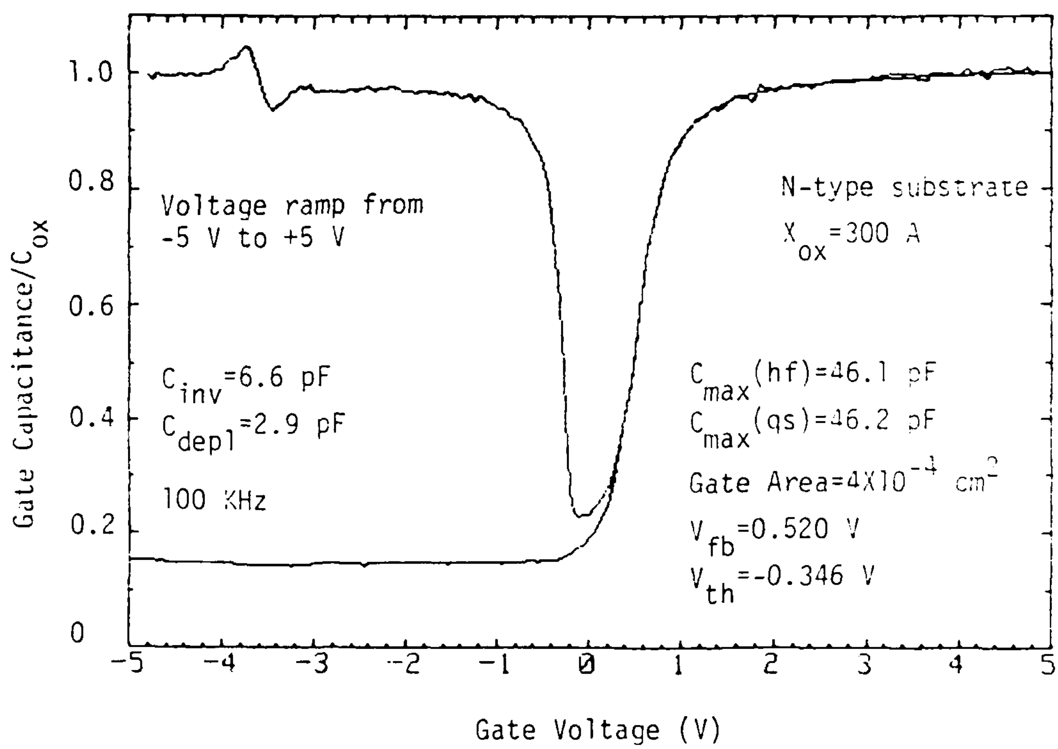
Gate Capacitance/C_{ox}
1.0
0.8
0.6
0.4
0.2
0
-5
-4
-3
-2
-1
0
1
2
3
4
5
Gate Voltage (V)
Voltage ramp from
-5 V to +5 V
C_{inv}=6.6 pF
C_{depl}=2.9 pF
100 KHz
N-type substrate
X_{ox}=300 A
C_{max}(hf)=46.1 pF
C_{max}(qs)=46.2 pF
Gate Area=$4X10^{-4}$ cm^2
V_{fb}=0.520 V
V_{th}=-0.346 V

Figure 2

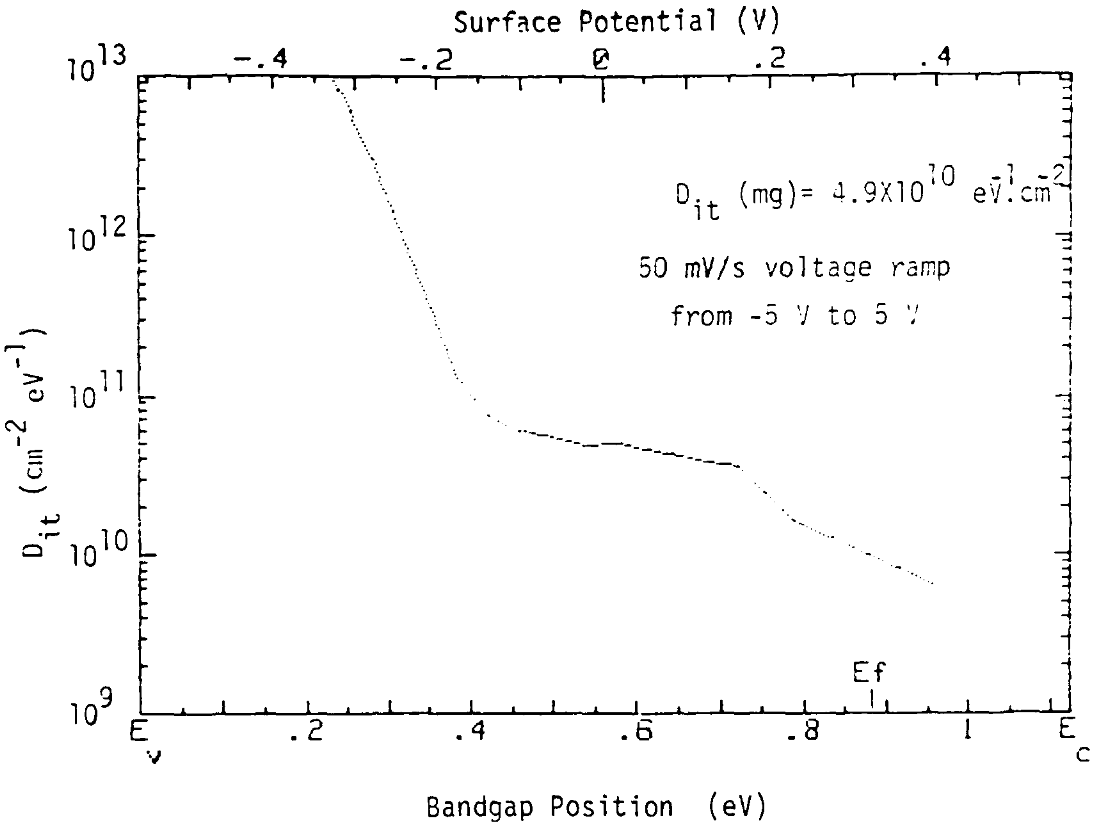
Surface Potential (V)
-.4
-.2
0
.2
.4
10^13
10^12
10^11
10^10
10^9
D_it (cm^-2 eV^-1)
D_it (mg)= 4.9X10^10 eV^-1.cm^-2
50 mV/s voltage ramp
from -5 V to 5 V
Ef
E_v
.2
.4
.6
.8
1
E_c
Bandgap Position (eV)

Figure 3

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